

REMARKS

Claim 27 has been amended. No new matter has been added. Claims 27-32 and 49-50 are currently pending in this application.

Claims 27, 49 and 50 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Kozicki, U.S. Patent Application Publication No. 2003/0035315 (Kozicki). This rejection is respectfully traversed.

Claim 27 recites an "array of resistance variable memory cells," "at least one memory cell comprising a pillar of stacked material layers on a semiconductor substrate, the stacked layers comprising a first electrode layer, a chalcogenide glass layer . . . and a second electrode layer, each layer having lateral edges, the lateral edges of each layer approximately vertically aligned with lateral edges of each other layer."

Kozicki relates to a microelectronic programmable structure for storing information. Kozicki discloses that his microelectronic programmable structure includes an ion conductor, which may be a chalcogenide glass with a metal dissolved therein, an electrode and a contact. Kozicki discloses that his microelectronic programmable structure can have several different configurations. However, none of Kozicki's configurations include "a pillar of stacked material layers on a semiconductor substrate, the stacked layers comprising a first electrode layer, a chalcogenide glass layer having metal ions diffused therein . . . and a second electrode layer, each layer having lateral edges, the lateral edges of each layer approximately vertically aligned with lateral edges of each other layer," as recited by independent claim 27.

The examiner points to Kozicki's figures 4 and 29 as showing the pillar structure recited in claim 27. Kozicki's figure 4, however, shows only an electrode 420, an ion conductor 440 and a diode 470 within a via. The electrode 430 is not within the

via and its lateral edges are not aligned with the lateral edges of the layers within the via. Kozicki's figure 29 shows programmable devices formed about a common electrode 2920. The ion conductor is formed within vias between the common electrode and a second electrode. Kozicki states that the second electrodes 2930-2936, 2938-2944 are bit lines or word lines. Kozicki at paragraph [0103]. The lateral edges of the common electrode 2920, the bit lines and word lines are not approximately vertically aligned with lateral edges of each other or the ion conductor. Therefore, Kozicki does not disclose the limitations of independent claim 27. For at least these reasons, withdrawal of this request is respectfully requested.

Claims 28-30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kozicki, in view of Wolstenholme et al, U.S. Patent Publication No. 5,751,012 (Wolstenholme).

As discussed above, Kozicki fails to disclose, teach or suggest all limitations of independent claim 27. To supplement certain deficiencies of Kozicki, the examiner relies on Wolstenholme. Like Kozicki, Wolstenholme fails to teach or suggest "a pillar of stacked material layers on a semiconductor substrate, the stacked layers comprising a first electrode layer, a chalcogenide glass layer having metal ions diffused therein . . . and a second electrode layer, each layer having lateral edges, the lateral edges of each layer approximately vertically aligned with lateral edges of each other layer," as recited by independent claim 27.

Instead, Wolstenholme relates to a polysilicon pillar diode for delivering current flow through a phase change-type resistance variable memory cell. Wolstenholme at Abstract. Wolstenholme's phase change -type resistance variable memory cell operates differently than Kozicki's programmable device and does not include an ion conductor. According to Wolstenholme, only the polysilicon diode is

formed as a pillar, not the memory cell. Thus, even when considered in combination, Kozicki and Wolstenholme fail to teach or suggest all limitations of independent claim 27.

Although Wolstenholme discloses a pillar, the pillar is a diode. Accordingly, there would be no motivation for one of ordinary skill in the art to modify Kozicki's programmable device with the structure of the pillar diode of Wolstenholme to achieve the claimed invention. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claims 31 and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kozicki, in view of Wolstenholme et al, U.S. Patent Publication No. 5,751,012 (Wolstenholme), and in further view of Shroff et al., U.S. Patent No. 6,515,343 (Shroff).

As discussed above, Kozicki and Wolstenholme, even when considered in combination, fail to disclose, teach or suggest all limitations of independent claim 27. Additionally, one of ordinary skill in the art would not be motivated to combine the teachings of Kozicki and Wolstenholme to achieve the claimed invention. Shroff relates to an antifuse memory and is cited for teaching a barrier layer. Shroff, however, is silent about any of the limitations of independent claim 27. Therefore, Shroff does not supplement the deficiencies of Kozicki or Wolstenholme. For at least these reasons, withdrawal of this rejection is respectfully requested.

Application No. 10/790,816
Amendment dated June 12, 2006
After Final Office Action of April 11, 2006

Docket No.: M4065.0607/P607-A

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Dated: June 12, 2006

Respectfully submitted,

By 

Thomas J. D'Amico

Registration No.: 28,371

Elizabeth Parsons

Registration No.: 52,499

DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP

2101 L Street NW

Washington, DC 20037-1526

(202) 785-9700

Attorneys for Applicant